PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	EMBEDDED PROCESSING/26/16334
1.3 Title of PCN	TSHT (China) subcontractor additional back-end qualification for 32, 64 and 128Kb I²C EEPROM in SO8N
1.4 Product Category	32, 64 & 128Kb I²C EEPROM in SO8N
1.5 Issue date	2026-05-13

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	
2.1.2 Phone	
2.1.3 Email	
2.2 Change responsibility	
2.2.1 Product Manager	
2.1.2 Marketing Manager	
2.1.3 Quality Manager	

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	N/A

4. Description of change		
	Old	New
4.1 Description	As announced in PCN 16143, the present PCN is the second step for the introduction of TSHT (China) subcontractor as a second source for assembly & test site of the low densities EEPROM I²C 1Kb to 128Kb in SO8N (in CMOS F8H+ process technology).	This PCN is then concerning the 32Kb, 64Kb and 128Kb.
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	- Form: Marking change, dot at pin 1, no ejector mark at bottom side, appearance of the leads - Fit: No change - Function: No change	

5. Reason / motivation for change	
5.1 Motivation	The strategy of the STMicroelectronics Memory division is to support our customers on products and service quality on a long-term basis. In line with this commitment, the qualification of the TSHT back-end assembly & test site as a second source will allow us to increase capacity and reinforce long term competitiveness. This PCN is coupled with matte Tin SO8N Shenzhen PCN (16335).
5.2 Customer Benefit	DOUBLE SOURCING

6. Marking of parts / traceability of change	
6.1 Description	N/A

7. Timing / schedule	
7.1 Date of qualification results	2026-09-14
7.2 Intended start of delivery	2026-09-14
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation	
8.1 Description	16334 RRCS2505 Reliability report F8H SO8N TSHT CuPd.pdf

8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2026-05-13

9. Attachments (additional documentations)
16334 Public product.pdf 16334 PCN TSHT 32 64 128 I2C F8H+.pdf 16334 RRCS2505 Reliability report F8H SO8N TSHT CuPd.pdf 16334 TERCS2026W16.pdf

10. Affected parts		
10. 1 Current		**10.2 New (if applicable)**
10.1.1 Customer Part No	**10.1.2 Supplier Part No**	**10.1.2 Supplier Part No**
	M24128-BFMN6TP	
	M24128-BRMN6TP	
	M24128-BWMN6TP	
	M24C32-FMN6TP	
	M24C32-RMN6TP	
	M24C32-WMN6TP	
	M24C64-FMN6TP	
	M24C64-RMN6TP	
	M24C64-WMN6TP	

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Public Products List

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PCN Title : TSHT (China) subcontractor additional back-end qualification for 32, 64 and 128Kb I²C EEPROM in SO8N

PCN Reference : EMBEDDED PROCESSING/26/16334

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

M24C32-FMN6TP	M24128-BFMN6TP	M24128-BRMN6TP
M24C64-WMN6TP	M24C32-RMN6TP	M24C64-RMN6TP
M24C32-WMN6TP	M24C64-FMN6TP	M24128-BWMN6TP

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Testing Evaluation Report / CS2026W16

TSHT (China) additional back-end qualification for 1Kb, 2Kb, 4Kb and 16Kb I²C EEPROM in SO8N

General Information	
Commercial Product	See appendix 1
Package	SO8N
Silicon Technology	CMOSF8H+
Division	MDRF / CS - Memory

Traceability	
Diffusion Plant	ST Rousset, France
Testing Evaluation result	
Pass	☒
Fail	☐

Release	Date	Author	Function
Rev 01	April the 2nd,2026	M.CAPELLE	Division Product Engineer

DOCUMENT APPROVERS:

M	Function	Location	Date
M. Lopez	Product Engineering Manager	Rousset, France	April 14th 2026
F. Roulet	NPI Engineering & Product Industrialization Director	Rousset, France	April 14th 2026

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TESTING EVALUATION OVERVIEW

- **GOAL**

The strategy of the STMicroelectronics Memory division is to support our customers on products and service quality on a long-term basis. In line with this commitment, the qualification of the TSHT back-end assembly & test site as a second source will allow us to increase capacity and reinforce long term competitiveness.

This testing evaluation report summarizes results from Final Test step qualification activities performed.

- **CONCLUSION**

All testing trials have been completed with results meeting expectations.
As such, the new products (see appendix1) manufactured in the ST Rousset 8", France (Diffusion plant) and assembled on TSHT (China) line have successfully passed testing evaluation.

Items	Status
Yield and bin pareto	PASS
Parametric correlation	PASS
HW qualification	PASS

1. PREREQUISITE

Production final test sequence description:

- Singulated test
- 100% test at room temperature (FT1) and sampling (QA-sampling)

This test report display data on few test vehicles that are covering all Commercial products involved in this change (appendix 3.1).

2. FINAL TEST RESULTS

2.1. Yield and bin pareto.

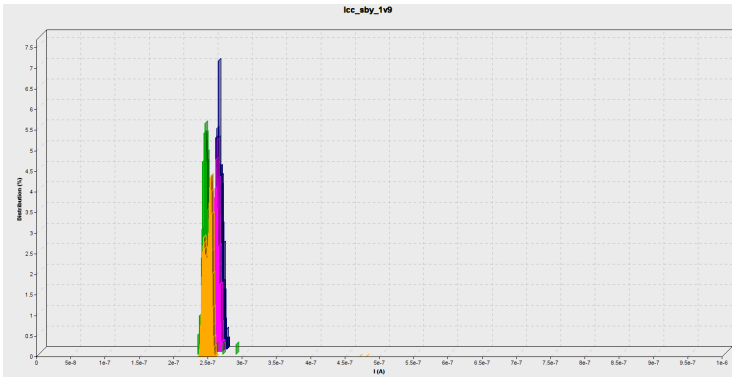
The qualification lots have been tested with the production test program and HW, 100% FT1 and QA-sampling. The test results are at the level of expectation, with good FT yield and no QA rejects.

Commercial Products	QTY_IN	QTY_out	FT_YIELD	Open*	Retention	Functionnal test	Iccsby	Short	BIN9/Marking
M24C01-WMN6TP	10045	9974	99.3%	0.5%	0.0%	0.0%	0.0%	0.0%	0.2%
M24C01-xxxx **REF**	426k	424k	99.7%	0.3%	0.04%	0.0%	0.0%	0.0%	NA
M24C02-WMN6TP	10062	10000	99.4%	0.4%	0.1%	0.0%	0.0%	0.0%	0.1%
M24C02-xxxx **REF**	11.8M	11.77M	99.8%	0.2%	0.03%	0.0%	0.0%	0.0%	NA
M24C04-FMN6TP	10049	9885	98.4%	1.3%	0.2%	0.0%	0.0%	0.0%	0.2%
M24C04-RMN6TP	10085	10000	99.2%	0.4%	0.2%	0.0%	0.0%	0.0%	0.2%
M24C04-WMN6TP	10146	10053	99.1%	0.6%	0.1%	0.0%	0.0%	0.0%	0.3%
M24C04-xxxx **REF**	12.7M	12.66M	99.8%	0.2%	0.04%	0.0%	0.0%	0.0%	NA

** Open rejects have been confirmed contact issue.*

2.2. Parametric correlation

The correlation between TSHT plant test results and the reference plant (ST Shenzhen) have been studied on the Icc standby. This parameter of interest is a datasheet parameter. No significant drift has been observed between TSHT plant and the reference.



	ICCSBY 1v9	Units	Median (nA)	Std dev (nA)
	Reference lot 1	5k	243.1	4.7
	Reference lot 2	21.4 k	252.7	5.1
	Reference lot 3	21.4 k	254.6	3.9
	New plant lot	81.9k	249.4	5.1

2.3 HW qualification

- Loop 100x the same units : parametric drift is aligned with tester accuracy, not test time deviation, good repeatability. **PASS**
- Test of reference plant rejects : rejected with TSHT test solution too. **PASS**

3. APPENDIX

3.1. APPENDIX 1: Details of product test vehicles and qualified products

Qualified products
M24C01-RMN6TP M24C01-WMN6TP M24C02-FMN6TP M24C02-RMN6TP M24C02-WMN6TP M24C04-FMN6TP M24C04-RMN6TP M24C04-WMN6TP M24C16-FMN6TP M24C16-RMN6TP M24C16-WMN6TP

4. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description

5. REVISION HISTORY

Release	Date	Description
		Initial release

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PRODUCT / PROCESS CHANGE NOTIFICATION

TSHT (China) subcontractor additional back-end qualification for 32, 64 and 128Kb I²C EEPROM in SO8N

What is the change?
As announced in PCN 16143, the present PCN is the second step for the introduction of **TSHT (China) subcontractor** as a second source for **assembly & test site** of the low densities EEPROM I²C 1Kb to 128Kb in SO8N (in CMOS F8H+ process technology). This PCN is then concerning the **32Kb, 64Kb and 128Kb.**

Why?
The strategy of STMicroelectronics is to support our customers on products and service quality on a long-term basis. In line with this commitment, the qualification of the TSHT back-end assembly & test site as a second source will allow us to increase capacity and reinforce long term competitiveness.
This PCN is coupled with matte Tin SO8N Shenzhen PCN (16335).

When?
Qualified samples will be available from Week 38 / 2026.
Shipment will start from Week 38 / 2026.

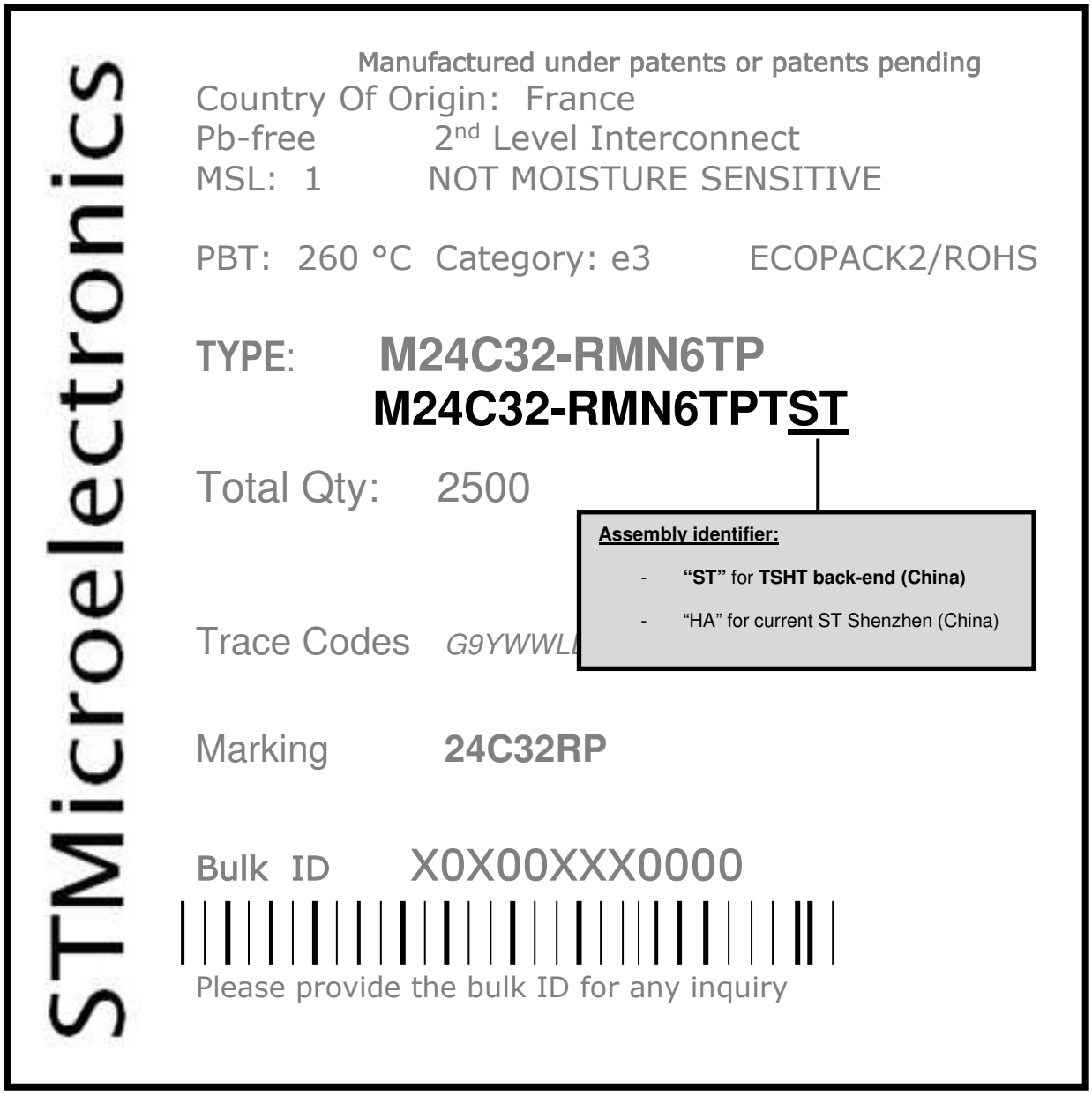
How will the change be qualified?
This change is qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability.
The Reliability Evaluation Report **RRCS2505** for 1Kb, 2Kb, 4Kb and 16Kb is available.
The report updated with additional products 32Kb, 64Kb and 128Kb will be available Week 38 / 2026.
The Test Evaluation Report **TERCS2026W16** for 1Kb, 2Kb, 4Kb and 16Kb is available.
The updated report with additional products 32Kb, 64Kb and 128Kb will be available Week 38 / 2026.

What is the impact of the change?
- **Form:** Marking change
- **Fit:** No change
- **Function:** No change

- ***BOX LABEL MARKING***

On the BOX LABEL, the difference is visible inside the **Finished Good Part Number** where the "**Assembly plant**" identifier is "**ST**" for products assembled & tested at the **additional TSHT (China) subcontractor**, this identifier being "HA" for current ST Shenzhen (China).

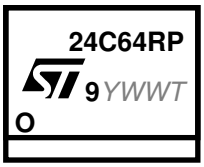
Example for M24C32-RMN6TP



How can the change be seen?

- DEVICE MARKING

The difference is visible inside the trace code (*PYWWT*) where the first digit "*P*" for the **assembly plant** identifier is "**9**" for the **additional TSHT (China) assembly & test subcontractor**, this identifier being "K" for the current ST Shenzhen (China).

	TSHT (China)	ST Shenzhen (China)
SO8N Example: *M24C64-RMN6TP*		

P = Assembly plant
Y = Last digit of the Year of Assembly
WW = Assembly Week
T = Process technology code/ Wafer Fab ID

Appendix A- Product Change Information

Product family / Commercial products:	32, 64 & 128Kb I²C EEPROM in SO8N
Customer(s):	All
Type of change:	Additional back-end site
Reason for the change:	Additional sourcing
Description of the change:	TSHT (China) subcontractor additional back-end to current ST Shenzhen (China) for 32, 64 & 128Kb CMOSF8H+ I²C EEPROM
Forecast date of the change: (Notification to customer)	Week 20 / 2026
Forecast date of Qualification samples availability for customer(s):	Week 38 / 2026
Qualification Report availability:	Reliability Evaluation Report **RRCS2505** for 1Kb, 2Kb, 4Kb and 16Kb is available. Updated report with additional products 32Kb, 64Kb and 128Kb will be available Week 38 / 2026. Test Evaluation Report **TERCS2026W16** for 1Kb, 2Kb, 4Kb and 16Kb is available. Updated report with additional products 32Kb, 64Kb and 128Kb will be available Week 38 / 2026.
Marking to identify the changed product:	*Assembly plant identifier "**9**" on SO8N package.*
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Estimated date of first shipment:	Week 38 / 2026

Appendix B: concerned Commercial Part Numbers:

Commercial product	Finished Good Part number	Qualified samples availability
M24C32-FMN6TP	M24C32-FMN6TPTST	Week 38 / 2026
M24C32-RMN6TP	M24C32-RMN6TPTST	Week 38 / 2026
M24C32-WMN6TP	M24C32-WMN6TPTST	Week 38 / 2026
M24C64-FMN6TP	M24C64-FMN6TPTST	Week 38 / 2026
M24C64-RMN6TP	M24C64-RMN6TPTST	Week 38 / 2026
M24C64-WMN6TP	M24C64-WMN6TPTST	Week 38 / 2026
M24128-BFMN6TP	M24128BFMN6TPTST	Week 38 / 2026
M24128-BRMN6TP	M24128BRMN6TPTST	Week 38 / 2026
M24128-BWMN6TP	M24128BWMN6TPTST	Week 38 / 2026

Appendix C: BOM comparison:

	TSHT subcon	ST Shenzhen
Leadframe	**Matte Tin post plating**	PPF 4-layer NiPdAgAu
Molding compound	**HITACHI CEL 9220**	SUMITOMO G700K
Glue die-attach	**HITACHI EN 4900** (PFAS free)	ABLESTIK 8611
Wire	**CuPd**	Cu

Document Revision History

Date	Rev.	Description of the Revision
May 11, 2026	1.00	Christian POLI - First draft creation

Source Documents & Reference Documents

Source document Title	Rev.:	Date:

RRCS2505 - Reliability Report

New Back End site qualification

F8H+ SO8N TSHT CuPd

General Information	
Commercial Product	M24C01-RMN6TP M24C01-WMN6TP M24C02-FMN6TP M24C02-RMN6TP M24C02-WMN6TP M24C04-FMN6TP M24C04-RMN6TP M24C04-WMN6TP M24C16-FMN6TP M24C16-RMN6TP M24C16-WMN6TP
Product Line	3FE41T, 24161T
Package	SO 08 .15 JEDEC
Silicon Technology	CMOSF8H+

Traceability	
Diffusion Plant	Rousset 8
Assembly Plant	TSHT- TianShui HuaTian-China

Reliability Assessment	
Pass	x
Fail	

Release	Date	Author	Function
1.0	Sept 18th 2025	Michel DERIE	CS Back-End quality Manager

DOCUMENT ACTORS:

Name	Function	Location	Date
Michel DERIE	CS Back-End quality Manager	Rousset	Sept 18th 2025
Nicolas DUMONT	CS Product Qualification and Reliability Manager	Rousset	Sept 18th 2025

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RELIABILITY EVALUATION OVERVIEW

- **OBJECTIVE**

The aim of this reliability is to qualify the new TSHT assembly site for F8H technology EEPROM ICs for SO8N package.

Scope:

- F8H technology serial EEPROM products with memory size 1 to 16k
- Package SO8N
- Wire type CuPd

- **CONCLUSION**

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Package oriented tests have not put in evidence any criticality.

Based on the overall results obtained, F8H technology EEPROM products with memory size 1 to 16k, assembled in SO8N package using TSHT plant have positively passed reliability evaluation.

TABLE OF CONTENT

1. RELIABILITY STRATEGY

Reliability evaluation is based on the standard STMicroelectronics corporate procedures for quality and reliability, namely RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION, and in compliance with the JESD-47K international standard.

The following qualification strategy has been defined:

• Package reliability evaluation on 3 assembly lots of F8H technology.

Reliability trials performed as part of this reliability evaluation are listed in test results summary in section 3, including specifications references

2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1. Generalities

The 3 lots used for qualification are 4k product.

2.2. Traceability

2.2.1.Wafer Fab Information

Main die - S3FE41TA

Wafer Fab Information	
FAB1	
Wafer fab name / location	ST SAS Rousset / Rousset 8
Wafer diameter (inches)	8
Wafer thickness (µm)	280
Silicon process technology	CMOSF8H+
Die finishing front side (passivation) materials	USG NitUV (HFP USG UV Nitride)
Die finishing back side Materials	RAW SILICON - BACK GRINDING
Stepping die size (µm)	582, 604
Sawing street width (X,Y) (µm)	60,80

2.2.2.Assembly information

-Assembly Information	
Package 1:SO 08 .15 JEDEC	
Assembly plant name / location	TSHT / SC-Tian Shui Hua Tian-China
Die thickness after back-grinding (µm)	280µ
Die sawing method	Mechanical
Lead frame/Substrate material/supplier/reference	SO8 70x70 (HTBJ)
Lead frame finishing (material/thickness)	Ag Spot
Die attach material/type(glue/film)/supplier	EN-4900GC
Wire bonding material/diameter/supplier	0.8mil PdCu
Molding compound material/supplier/reference	CEL-9220HF10TS
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL1

3. TEST RESULTS SUMMARY

3.1. Reliability testing information

Reliability Testing Information	
Reliability laboratory name / location	Grenoble Rel Lab, Rousset MDG Rel Lab , TSHT reliability lab

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3.2. Lot information

SO8N

Lot #	Diffusion Lot	Assy Lot	Raw Line	Package
Lot 1	G450705	G9522168	TSO7*2404FTA	SO 08 .15 JEDEC
Lot 2	G450553	G9522159	TSO7*2404FTA	SO 08 .15 JEDEC
Lot 3	G450554	G9522156	TSO7*2404FTA	SO 08 .15 JEDEC

3.3. Test plan and results summary

ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, T&H 168h 85°C/85%RH 3x Reflow simulation Peak Reflow Temp= 260°C ☒ Testing at Room T°	3	231	693	Lot 1 : 0/231 Lot 2 : 0/231 Lot 3 : 0/231	
HTSL	JESD22-A103	Ta= 150°C Duration= 1000h ☒ Testing at Room T°	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
TC	JESD22-A104	Ta= -65 / +150°C, 2cy/h Duration = 500cy ☒ After PC ☒ Testing at Room T°	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
HAST	JESD22-A118	Ta=130°C/85%RH + bias 5.6V Duration= 96h ☒ After PC ☒ Testing at Room T°	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
UHAST	JESD22-A118	Ta=130°C/85%R Duration= 96h ☒ After PC ☒ Testing at Room T°	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	

Electrical Verification Tests

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CDM	JS-002	3u/ voltage: 250, to 1500V by step of 250V total 18u ☒Testing at Room T°	3	18	54	Lot 1 : 0/18 Lot 2 : 0/18 Lot 3 : 0/18	Gating= 500V

Package Assembly Integrity Tests

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PD	Internal	Dimensions measurement vs POA	3	10	30	PASS	
SD	J-STD-002D	2 conditions ☒ Dry (150℃,8H) SnAgCu ☒ Steam (85 ℃/85%RH,8H) SnAgCu	3	20	60	PASS	
WBP	MIL-STD883 Method 2011	EQUIPMENT: Dage BT4000 SAMPLING: 30 wires / 6 units (5 wires /unit) ☒ Testing at T0 after package opening	3	30	90	PASS	
WBS	JESD22-B116	EQUIPMENT: Dage BT4000 SAMPLING: 30 wires / 5 units (6 wires /unit) ☒ Testing at T0 after package opening	3	30	90	PASS	

Note: Test method revision reference is the one active at the date of reliability trial execution.

4. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47-L	Stress-Test-Driven Qualification of Integrated Circuits

5. GLOSSARY

CDM	Electrostatic Discharge - Charged device model
HAST	Biased HAST (Highly Accelerated Stress Test)
HBM	Electrostatic Discharge - Human Body Model
HTSL	High Temperature Storage Life
PC	Preconditioning
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
WBS	Wire Bond Shear
WBP	Wire Bond Pull
PD	Physical Dimensions
SD	Solderability

6. REVISION HISTORY

Release	Date	Description
1.0	Sept 19th 2025	Initial release

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